Applied Brain Research

Intelligence. No connection required.

DAC - AI on the Edge Roundtable

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ABR Edge Experience

ABR Edge Successes

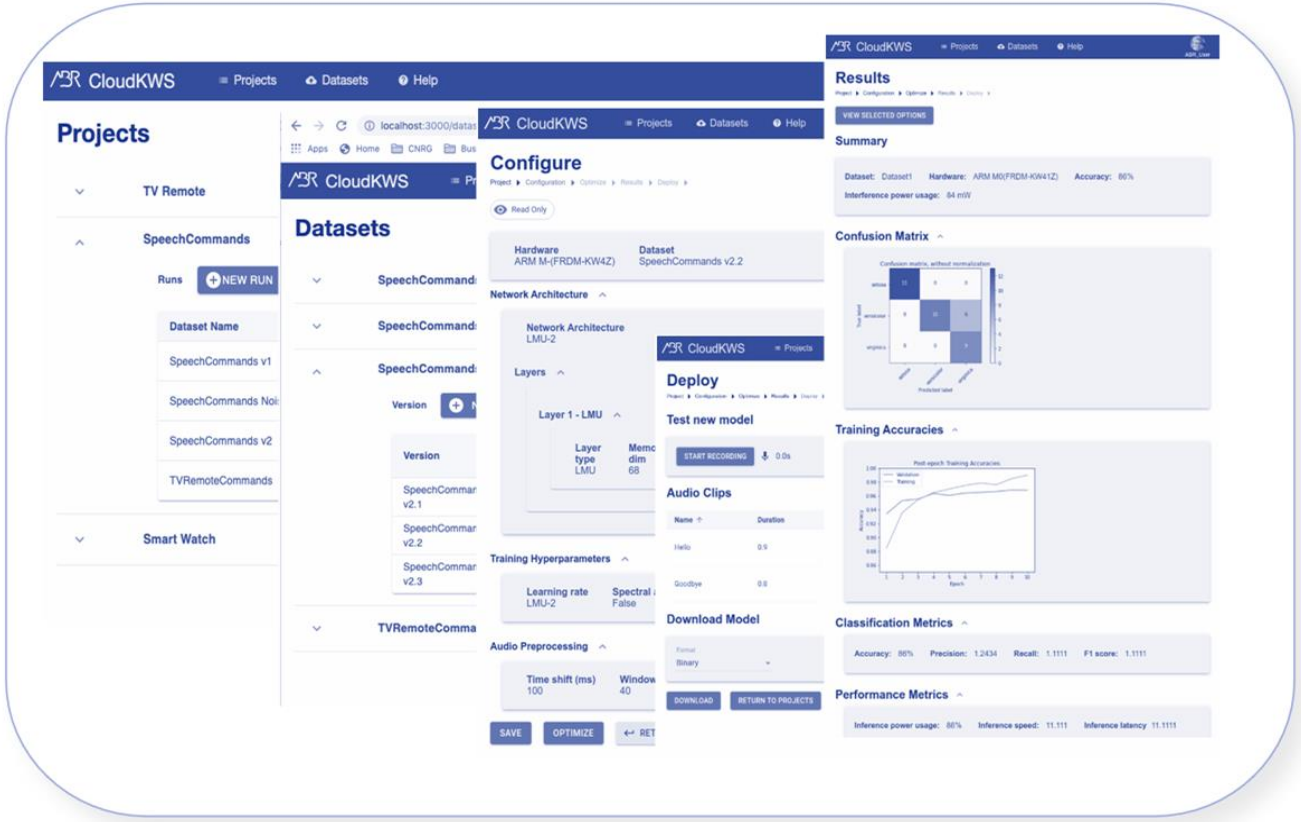
- Record setting extreme edge implementations for keyword spotting
  - ARM M4 (2% accuracy, 10x latency)
  - Intel Loihi neuromorphic chip (5x power)

Full Stack SaaS

- No-code model development
- State-of-the-art accuracy, size, power

Now

- **New chip**



Key Technical Challenge

ABR

Challenge

- Better AI ⇒ larger AI
- Larger AI ⇒ more memory
- ∴ Memory density is critical

- Large memory ⇒ large leakage

How do you get large memory with low power?

Solution

1. 2x memory reduction from LMU

1. MRAM
   - Better memory density
   - Non-volatile
   - Slow (no problem)
   - Write longevity (no problem)

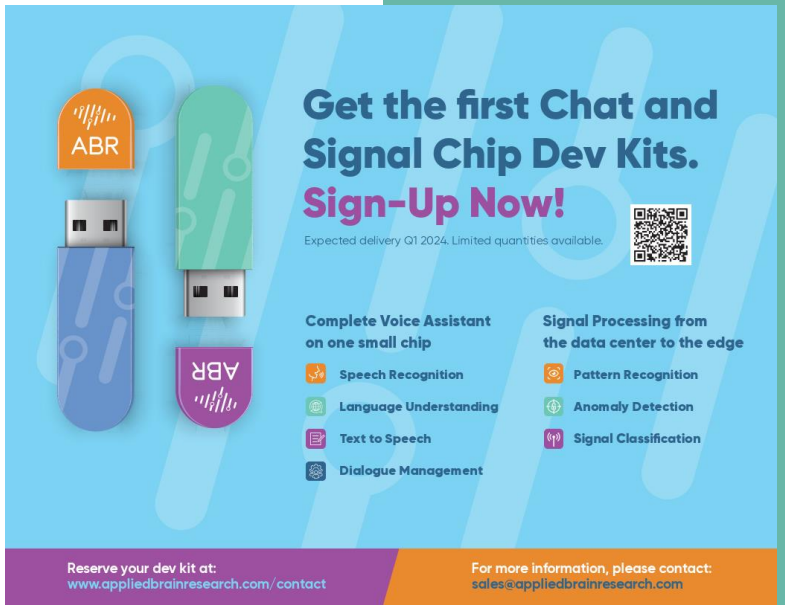
Result: 100x low power for real-time large-scale AI

Key Markets

ChatChip

- Mobile full speech/dialog
- Automatic captioning
- Language modeling
- Audio environment monitor
- On-device voice manuals
- High-privacy full voice
- In-ear translation

MPW Nov 23
Dev Kit Q1-24



SignalChip

- Wearables
- Heartbeat, breathing, other biosignals
- Predictive maintenance
- Signal prediction (control)
- Anomaly detection
- Advanced noise suppression

ABR's Time Series Processing (TSP) chip family

Problem

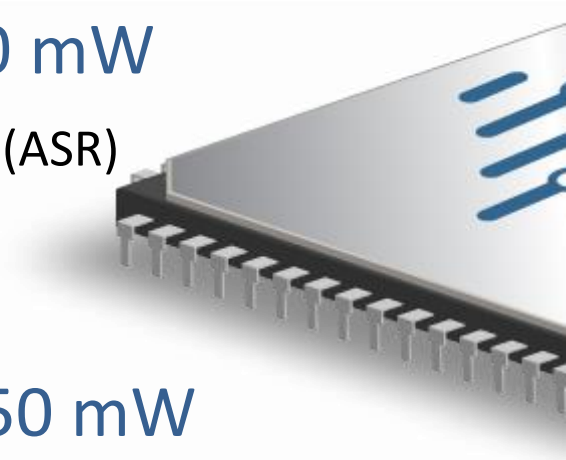
Current chips <100 mW

- Keywords
- Key phrases
- Simple event detection

Solution

ABR's ChatChip < 50 mW

- Full Speech Recognition (ASR)
- Language Models
- Text-to-speech



ABR's SignalChip < 50 mW

- Biosignal processing
- Difficult anomaly detection
- Sophisticated noise filtering

ABR enables previously unachievable edge applications

Proprietary advantage

ABR's Legendre Memory Unit (LMU)

ABR

The LMU makes large-scale time series AI at the edge possible

ABR TSP1445

ABR Time Series Processor (TSP)

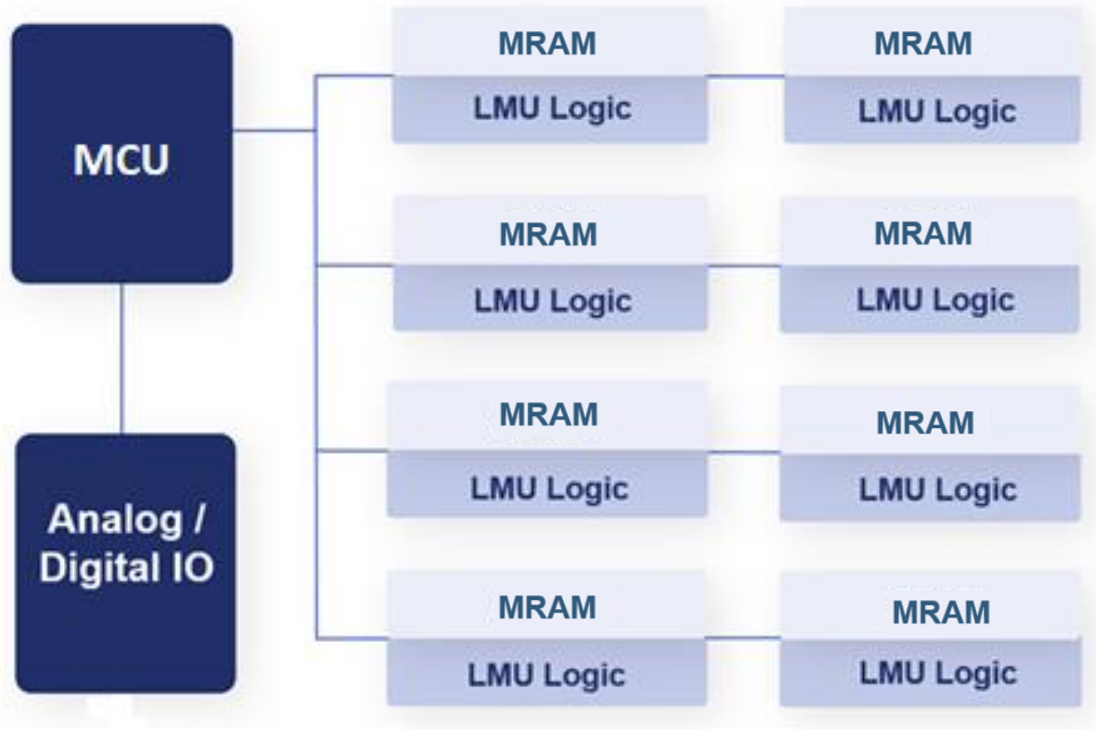
- Power < 100µW idle < 50mW
  for full Automatic Speech Recognition (ASR)
- 22nm standard digital process
- MRAM for low size and power

Integration

- UART, GPIO, SPI, QSPI
- PDM/I²S interface

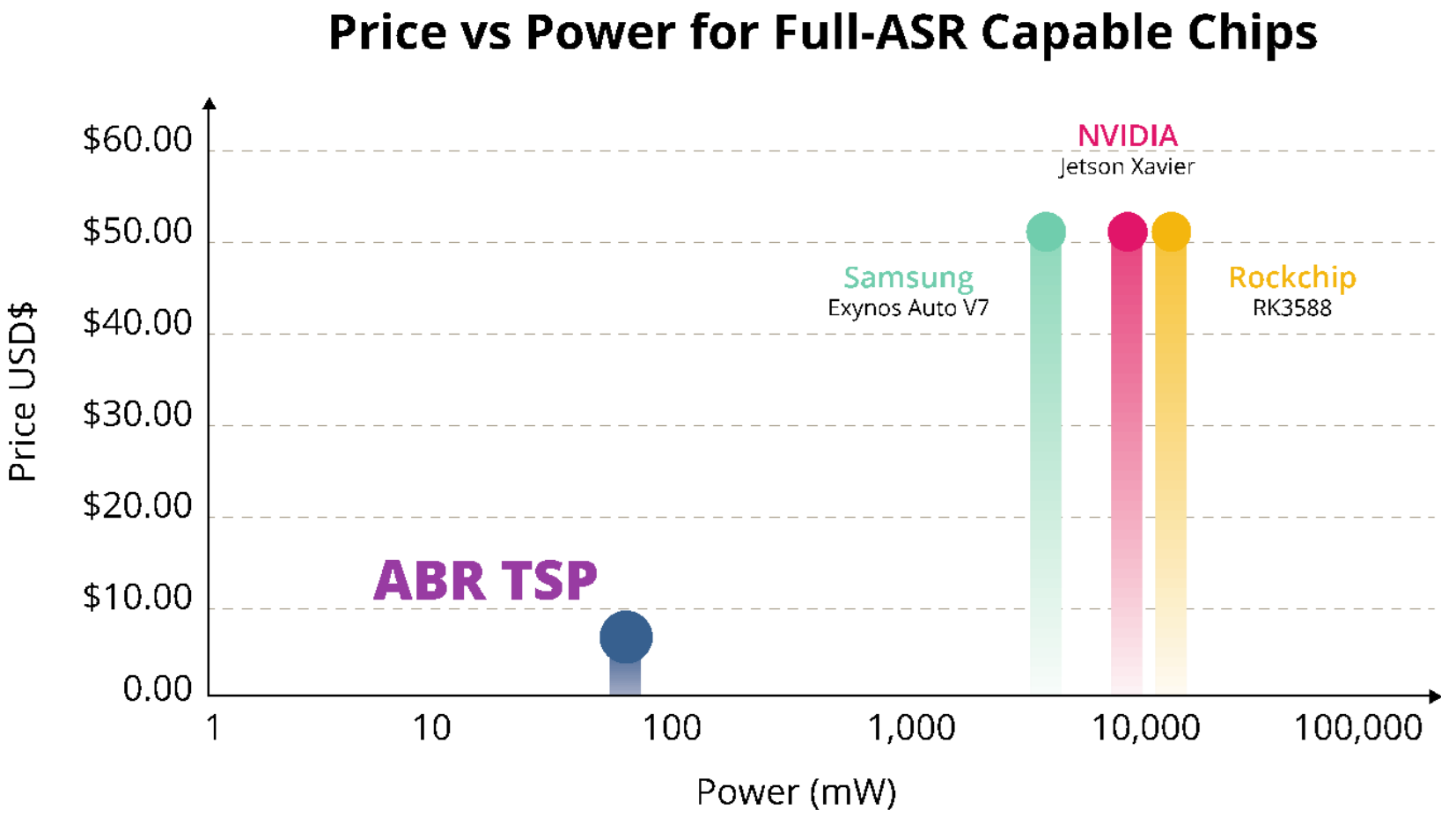
Design and tapeout

- **ABR** designed RTL and compiler
- November 2023 MPW tapeout, TSMC



ABR's TSP delivers large AI performance

The Lowest Cost and Power of full-ASR Capable Chips



David Kanter, CEO, MLCommons

There are no benchmarks for this power and capability.

Sources: Published data, where none available, ABR estimates use information such as chip area and demo-board pricing.

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